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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/941,484	08/28/2001	Ali Muhtaroglu	42390.P10961	6234

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EXAMINER

TABONE JR, JOHN J

ART UNIT PAPER NUMBER

2133

DATE MAILED: 08/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/941,484

Applicant(s)

MUHTAROGLU, ALI

Examiner

John J. Tabone, Jr.

Art Unit

2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 12 July 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-11,26,28-30 and 32-43 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-11,26,28-30 and 32-43 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

### DETAILED ACTION

1. Pending claims 1-11, 26, 28-30, and 32-43 have been examined.
2. Applicant's arguments with respect to claims 1, 26, 30, and 40 have been considered but are moot in view of the new ground(s) of rejection.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1, 2, 4, 26, 29, 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Andrews (US-5,231,314), hereinafter Andrews, in view of Yang et al. (US-6310571) hereinafter Yang.

#### Claim 1:

Andrews teaches the respective voltage signals from the DAC (voltage generator) and ramp generator RAMP (reference voltage) are applied at the first and second inputs of a voltage comparator COMP (sense amplifier). The output of the voltage comparator provides the desired signal STB. Andrews also teaches the boundary scan cells BSC of the boundary scan register TDR1 are not shown on the IC chip block diagram except at the STS input pin and STB output

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pin. Figure 8 shows the output of the voltage comparator COMP (sense amplifier) is connected to the output boundary scan cells BSC STB (boundary scan register). (See col. 5, lines 42-49; col. 6, lines 12-17; Figure 8). Andrews does not explicitly teach "an externally supplied reference voltage". However, Andrews does teach the ramp generator RAMP (reference voltage) is connected to the STS input through boundary scan cells of the boundary scan register TDR1. Yang teaches comparators 16a-n are controlled by external control signal RAMP. (Col. 1, lines 63-65, Fig. 2). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Andrews' RAMP generator (reference voltage) and voltage comparator COMP (sense amplifier) to incorporate Yang's external RAMP generator and comparator 16a. Yang's externally generated RAMP signal is coupled to the inverting input of the comparator 16a. The artisan would have been motivated to do so because it would save chip area and add more flexibility to Andrews' chip. The artisan also, would have been motivated to do so because Andrews would not be limited to a particular type of circuit for generating a RAMP signal.

Claim 2:

Andrews teaches the test access port TAP of the IC device of FIG. 5 incorporates as one of the design specific registers a controllable timing circuit design specific TAP data register TDR6 referred to herein as CTC/DS/TDR which capable of receiving and temporarily storing any of 256 different CTC digital timing codes (configuration bits). Andrews further discloses the output of the CTC/DS/TDR is coupled to a digital to analog converter DAC that converts the

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256 digital timing codes into 256 respective graduated analog voltage levels at the output of the DAC. (See col. 5, lines 50-68).

Claim 26 and 30:

The claim limitations of a voltage generator, sense amplifier and a boundary scan register (logic) coupled to the sense amplifier are rejected per claim 1. The claim limitation of logic to apply a set of configuration bits is rejected as per claim 2 above.

Claims 4 and 29:

Per the rejection of claim 2, Andrews teaches the voltage generator is a digital-to-analog converter (DAC).

4. Claims 3, 5, 6, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Andrews (US-5,231,314), hereinafter Andrew, in view of Yang et al. (US-6310571) hereinafter Yang, further in view of Taylor (US-6,085,345), hereinafter Taylor.

Claims 3 and 28:

Andrews does not explicitly teach of a switch coupled between the voltage generator (DAC) and the sense amplifier (voltage comparator COMP), however, Andrews does teach of the coupling of the DAC the non-inverting input of the COMP. (See col. 6, lines 12-14; Fig. 8). Taylor teaches a pass gate multiplexer 60 which allows a voltage to be alternatively driven from a digital-to-analog converter (DAC) 62. (See col. 5, lines 37-39). It would have been obvious to one of ordinary skill in the art at the time the invention was made to replace Andrews'

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DAC with Taylor's DAC 62 and pass gate multiplexer 60 combination. The artisan would be motivated to do so because it would enable Andrews to open and close the connection to the non-inverting input of the voltage comparator COMP.

Claim 5:

The motivation for modifying Andrews with Taylor's switch is rejected as per claims 3 and 28 above. Taylor suggests the DAC 62 and test signal 61 may be controlled through a boundary scan register (second logic). (See col. 5, lines 62-67; col. 6, lines 1-5).

Claim 6:

Taylor suggests the second logic may be boundary scan registers.

5. Claims 7, 40-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Andrews (US-5,231,314), hereinafter Andrew, in view of Taylor (US-6,085,345), hereinafter Taylor, further in view of Bates et al. (US-6,477,674), hereinafter Bates, and further in view of Yang et al. (US-6310571) hereinafter Yang.

Claim 7:

Andrews does not explicitly teach the use of an I/O loop back compare circuit coupled to the sense amplifier, however, Andrews teaches the boundary scan cells BSC of the boundary scan register TDRI are not shown on the IC chip block diagram except at the STS input pin and STB output pin. Figure 5 shows the output of the voltage comparator COMP (sense amplifier) is connected to the output BSC STB. (See col. 5, lines 42-49; col. 6, lines 12-17; Figure 5). Bates

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teaches an I/O test circuit 110 that includes a delay unit 203, a MUX 205, a test pattern generator 210 (loop back pattern generator), a stage unit 215, a compare unit 220, a MUX 225 and a latch 230. Delay unit 203 provides a delay of core clock signals received at I/O test circuit 110 for operation in the AC loopback testing mode. Bates also teaches test pattern generator 210 is coupled to MUX 205 and MUX 115, and is used to generate test pattern signals for testing I/O test circuit 100 upon the initiation of a loopback test. Bates further discloses in one embodiment, latch 230 is a boundary scan latch as described in the Institute of Electrical and Electronics Engineers (IEEE) 1149.1 Specification. Latch 230 is subsequently examined as a part of a boundary scan chain. (See col. 3, lines 19-25, 46-49; col. 4, 21-27; Fig. 2). It would have been obvious to one of ordinary skill in the art at the time the invention was made replace Andrews' boundary scan cells with Bate's I/O AC loopback test circuit. The artisan would be motivated to do so because it would enable Andrews to perform I/O loopback tests within the boundary scan cells and to load test pattern signals into test pattern generator 210 via a test chain prior to conducting a loopback test for the controlling of the switches.

Claim 40:

Andrews teaches the respective voltage signals from the DAC (voltage generator) and ramp generator RAMP (reference voltage) are applied at the first and second inputs of a voltage comparator COMP (sense amplifier). The output of the voltage comparator provides the desired signal STB. Andrews also teaches the boundary scan cells BSC of the boundary scan register TDRI are not



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shown on the IC chip block diagram except at the STS input pin and STB output pin. Figure 5 shows the output of the voltage comparator COMP (sense amplifier) is connected to the output BSC STB. (See col. 5, lines 42-49; col. 6, lines 12-17; Figure 5). Andrews does not explicitly teach the use of an I/O loop back compare circuit coupled to the sense amplifier, however, Andrews teaches the boundary scan cells BSC of the boundary scan register TDRI are not shown on the IC chip block diagram except at the STS input pin and STB output pin. Figure 5 shows the output of the voltage comparator COMP (sense amplifier) is connected to the output BSC STB. (See col. 5, lines 42-49; col. 6, lines 12-17; Figure 5). Bates teaches an I/O test circuit 110 that includes a delay unit 203, a MUX 205, a test pattern generator 210, a stage unit 215, a compare unit 220 (compare circuitry), a MUX 225 and a latch 230. Delay unit 203 provides a delay of core clock signals received at I/O test circuit 110 for operation in the AC loopback testing mode. Bates further teaches in one embodiment, latch 230 is a boundary scan latch as described in the Institute of Electrical and Electronics Engineers (IEEE) 1149.1 Specification. Latch 230 is subsequently examined as a part of a boundary scan chain. (See col. 3, lines 19-25; col. 4, 21-27; Fig. 2). It would have been obvious to one of ordinary skill in the art at the time the invention was made replace Andrews' boundary scan cells with Bate's I/O AC loopback test circuit. The artisan would be motivated to do so because it would enable Andrews to perform I/O loopback tests within the boundary scan cells and examine the results as part of the boundary scan chain. Andrews does not explicitly teach "an externally supplied reference voltage". However, Andrews does teach the ramp generator

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RAMP (reference voltage) is connected to the STS input through boundary scan cells of the boundary scan register TDR1. Yang teaches comparators 16a-n are controlled by external control signal RAMP. (Col. 1, lines 63-65, Fig. 2). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Andrews' RAMP generator (reference voltage) and voltage comparator COMP (sense amplifier) to incorporate Yang's external RAMP generator and comparator 16a. Yang's externally generated RAMP signal is coupled to the inverting input of the comparator 16a. The artisan would have been motivated to do so because it would save chip area and add more flexibility to Andrews' chip. The artisan also, would have been motivated to do so because Andrews would not be limited to a particular type of circuit for generating a RAMP signal.

Claim 41:

Andrews teaches the test access port TAP of the IC device of FIG. 5 incorporates as one of the design specific registers a controllable timing circuit design specific TAP data register TDR6 referred to herein as CTC/DS/TDR which capable of receiving and temporarily storing any of 256 different CTC digital timing codes (configuration bits). Andrews further discloses the output of the CTC/DS/TDR is coupled to a digital to analog converter DAC (levels generating circuit) that converts the 256 digital timing codes into 256 respective graduated analog voltage levels at the output of the DAC. (See col. 5, lines 50-68).

Claim 42:

Andrews does not explicitly teach of a switch coupled between the voltage generator (DAC) and the sense amplifier (voltage comparator COMP), however, Andrews does teach of the coupling of the DAC the non-inverting input of the COMP. (See col. 6, lines 12-14; Fig. 8). Taylor teaches a pass gate multiplexer 60 which allows a voltage to be alternatively driven from a digital-to-analog converter (DAC) 62. (See col. 5, lines 37-39). It would have been obvious to one of ordinary skill in the art at the time the invention was made to replace Andrews' DAC with Taylor's DAC 62 and pass gate multiplexer 60 combination. The artisan would be motivated to do so because it would enable Andrews to open and close the connection to the non-inverting input of the voltage comparator COMP.

Claim 43:

Per the rejection of claim 41, Andrews teaches the levels generating circuit is a digital-to-analog converter (DAC).

***Response to Amendment***

6. Applicant's arguments filed 7/12/2004 with respect to claims 8-11, 32-39 has been fully considered but they are not persuasive.

The Applicant contends, "Andrews is directed to testing integrated circuit timing, whereas embodiments of the present invention are directed to testing integrated circuit input levels. The Examiner would like to point out that by virtue of Andrews incorporating a voltage comparator COMP (sense amplifier) connected to a RAMP signal on the inverting input and the output of a DAC on the non-inverting input (See Fig. 8) constitutes a comparison of voltage levels

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and therefore tests levels of a chip "in the process" of testing the timing of an integrated circuit.

Assuming for the sake of argument that Andrews only tests the timing of an integrated circuit, the present invention claim language does not specifically disclose as being "directed to testing integrated circuit input levels". The Examiner cannot find this claim language in the preamble or body of any of the independent claims 1, 8, 26, 30, 33, 37, and 40. The Examiner would also like to point out that the M.P.E.P. (see M.P.E.P. 2111) requires that the Examiner give "the broadest reasonable interpretation" to the claims consistent with the specification", it also warns that "reading a claim in light of the specification, to thereby interpret limitations explicitly recited in the claim, is quite a different thing from reading limitations of the specification into the claim, to thereby narrow the scope of the claim by implicitly adding disclosed limitations which have no express basis in the claim." That is, the claims must stand on it's own.

The Examiner disagrees with the Applicant and maintains all rejections of the independent and dependent claims 8-11, 32-39 according to the last office action mailed April 8, 2004. These rejections are further repeated below for the Applicant's convenience.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to

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be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 8-11, 32, 33, 37 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Andrews (US-5,231,314), hereinafter Andrew, in view of Taylor (US-6,085,345), hereinafter Taylor.

Claims 8 and 33:

The claim limitations of a voltage generator, sense amplifier and a boundary scan register coupled to the sense amplifier are rejected per claim 1. Andrews does not explicitly teach of the use of “a structural tester coupled to the integrated circuit to apply a reference voltage to the inverting input of the sense amplifier”, however, Andrews does teach the ramp generator RAMP (reference voltage) is connected to the STS input through boundary scan cells of the boundary scan register TDR1. Taylor suggests that circuitry can be externally controlled by a logic tester (structural tester) during testing through the boundary scan logic. (See col. 5, lines 39-43, 62-67; col. 6, lines 1-5). It would have been obvious to one of ordinary skill in the art at the time the invention was made that a structural tester could be added to Andrew’s STS pin in order to apply reference signals. The artisan would be motivated to do so because this would lower the cost of using large Automatic Test Equipment and would enable the artisan to screen for manufacturing defects and ensure the manufacturing correctness of the device under test using DFT channels (boundary scan I/O).

Claims 9 and 32:

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Andrews teaches the test access port TAP of the IC device of FIG. 5 incorporates as one of the design specific registers a controllable timing circuit design specific TAP data register TDR6 referred to herein as CTC/DS/TDR which capable of receiving and temporarily storing any of 256 different CTC digital timing codes (configuration bits). Andrews further discloses the output of the CTC/DS/TDR is coupled to a digital to analog converter DAC that converts the 256 digital timing codes into 256 respective graduated analog voltage levels at the output of the DAC. (See col. 5, lines 50-68).

Claim 10:

Andrews does not explicitly teach of a switch coupled between the voltage generator (DAC) and the sense amplifier (voltage comparator COMP), however, Andrews does teach of the coupling of the DAC the non-inverting input of the COMP. (See col. 6, lines 12-14; Fig. 8). Taylor teaches a pass gate multiplexer 60 which allows a voltage to be alternatively driven from a digital-to-analog converter (DAC) 62. (See col. 5, lines 37-39). It would have been obvious to one of ordinary skill in the art at the time the invention was made to replace Andrews' DAC with Taylor's DAC 62 and pass gate multiplexer 60 combination. The artisan would be motivated to do so because it would enable Andrews to open and close the connection to the non-inverting input of the voltage comparator COMP.

Claim 11:

Per the rejection of claim 9, Andrews teaches the voltage generator is a digital-to-analog converter (DAC).

Claim 37:

The claim limitations of a voltage generator, sense amplifier, a boundary scan register coupled to the sense amplifier and a structural tester are rejected per claim 8 above. The claim limitations of a set of switches and second logic to open and close them are rejected per claim 5.

Claim 38:

Taylor suggests the second logic may be boundary scan registers.

8. Claims 33-36 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Andrews (US-5,231,314), hereinafter Andrew, in view of Taylor (US-6,085,345), hereinafter Taylor, further in view of Bates et al. (US-6,477,674), hereinafter Bates.

Claim 33:

The claim limitations of a voltage generator, sense amplifier, a boundary scan register coupled to the sense amplifier and a structural tester are rejected per claim 8 above. Andrews does not explicitly teach the use of an I/O loop back compare circuit coupled to the sense amplifier, however, Andrews teaches the boundary scan cells BSC of the boundary scan register TDRI are not shown on the IC chip block diagram except at the STS input pin and STB output pin. Figure 5 shows the output of the voltage comparator COMP (sense amplifier) is connected to the output BSC STB. (See col. 5, lines 42-49; col. 6, lines 12-17; Figure 5). Bates teaches an I/O test circuit 110 that includes a delay unit 203, a MUX 205, a test pattern generator 210, a stage unit 215, a compare unit 220 (compare circuitry), a MUX 225 and a latch 230. Delay unit 203 provides a delay

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of core clock signals received at I/O test circuit 110 for operation in the AC loopback testing mode. Bates further teaches in one embodiment, latch 230 is a boundary scan latch as described in the Institute of Electrical and Electronics Engineers (IEEE) 1149.1 Specification. Latch 230 is subsequently examined as a part of a boundary scan chain. (See col. 3, lines 19-25; col. 4, 21-27; Fig. 2). It would have been obvious to one of ordinary skill in the art at the time the invention was made replace Andrews' boundary scan cells with Bate's I/O AC loopback test circuit. The artisan would be motivated to do so because it would enable Andrews to perform I/O loopback tests within the boundary scan cells and examine the results as part of the boundary scan chain.

Claim 34:

The claim limitation of the voltage generator being responsive to a set of configuration bits is rejected as per claim 9 above.

Claim 35:

The claim limitation of a switch coupled between the voltage generator (DAC) and the sense amplifier (voltage comparator COMP) is rejected as per claims 3, 10 above.

Claim 36:

The claim limitation of voltage generator is a digital-to-analog converter (DAC) is rejected as per claim 11.

Claim 39:

Andrews does not explicitly teach the use of an I/O loop back compare circuit coupled to the sense amplifier, however, Andrews teaches the boundary



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scan cells BSC of the boundary scan register TDRI are not shown on the IC chip block diagram except at the STS input pin and STB output pin. Figure 5 shows the output of the voltage comparator COMP (sense amplifier) is connected to the output BSC STB. (See col. 5, lines 42-49; col. 6, lines 12-17; Figure 5). Bates teaches an I/O test circuit 110 that includes a delay unit 203, a MUX 205, a test pattern generator 210 (loop back pattern generator), a stage unit 215, a compare unit 220, a MUX 225 and a latch 230. Delay unit 203 provides a delay of core clock signals received at I/O test circuit 110 for operation in the AC loopback testing mode. Bates also teaches test pattern generator 210 is coupled to MUX 205 and MUX 115, and is used to generate test pattern signals for testing I/O test circuit 100 upon the initiation of a loopback test. Bates further discloses in one embodiment, latch 230 is a boundary scan latch as described in the Institute of Electrical and Electronics Engineers (IEEE) 1149.1 Specification. Latch 230 is subsequently examined as a part of a boundary scan chain. (See col. 3, lines 19-25, 46-49; col. 4, 21-27; Fig. 2). It would have been obvious to one of ordinary skill in the art at the time the invention was made replace Andrews' boundary scan cells with Bate's I/O AC loopback test circuit. The artisan would be motivated to do so because it would enable Andrews to perform I/O loopback tests within the boundary scan cells and to load test pattern signals into test pattern generator 210 via a test chain prior to conducting a loopback test for the controlling of the switches.

### ***Conclusion***

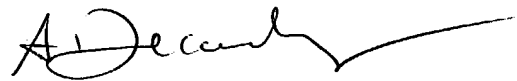
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Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (703) 305-8915. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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John J. Tabone, Jr.  
Examiner  
Art Unit 2133



ALBERT DECADY  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER